

1. A method of addressing imagers, comprising:
  - providing a bi-directional bus;
  - providing an array of imagers arranged in  $n$  rows and  $m$  columns wherein said  $n$  and  $m$  are positive integers, wherein  
5 each said imager is connected to said bi-directional bus, wherein each said imager has a Vmode terminal, wherein each said imager has a select terminal, and wherein each said imager can deliver a signal to said bi-directional bus only when a first selecting signal is applied to a Vmode  
10 terminal of that said imager and a second selecting signal is applied to a select terminal of that said imager simultaneously;
  - providing a first multiplexer having a vertical select input and  $n$  outputs, wherein each of said  $n$  outputs is  
15 connected to one of said Vmode terminals of said imagers;
  - providing a second multiplexer having a horizontal select input and  $n \times m$  outputs wherein each said output is connected to said select terminal of one of said imagers;
  - applying a vertical input signal to said vertical  
20 select input of said first multiplexer thereby producing said first selecting signal at one of said Vmode output lines; and
  - applying a horizontal input signal to said horizontal select input of said second multiplexer thereby

25 sequentially producing said second selecting signal at said  
select terminal of one of said imagers.

2. A method of accessing an imager array, said method  
comprising:

providing a bi-directional bus;

providing an array of imagers arranged in  $n$  rows and  $m$   
5 columns wherein said  $n$  and  $m$  are positive integers, wherein  
each said imager is connected to said bi-directional bus,  
and wherein a line of bits of any said imager is accessible  
by a line address;

initializing a column counter, a row counter, and said  
10 line address to zero; and

accessing all of said array wherein said accessing  
comprises further steps of:

accessing one line of one said imager  
corresponding to said line address, said column  
15 counter, and said row counter;

thereafter testing said column counter for  
equality to  $m-1$  wherein, if not equal, said column  
counter is incremented and said step of accessing one  
line is repeated and wherein, if equal, said column  
20 counter is reset;

thereafter testing said line address for equality  
to total lines in each said imager wherein, if not  
equal, said line address is incremented and said step  
of accessing one line is repeated, and wherein, if  
25 equal, said line address is reset; and

thereafter testing said row counter for equality  
to  $n-1$  wherein, if not equal, said row counter is  
incremented and said step of accessing one line is  
repeated, and wherein, if equal, said step of  
30 accessing all is completed.

3. The method according to Claim 2 wherein each said  
imager has a Vmode input and an output enable input and  
wherein said Vmode input and said output enable input must  
be enabled to allow said accessing.

4. The method according to Claim 3 wherein said  
column counter is multiplexed to generate a separate said  
output enable input for each said imager.

5. The method according to Claim 3 wherein said  
row counter is multiplexed to generate a said Vmode input  
for each said row of said imagers.

6. The method according to Claim 2 wherein said step of  
accessing one line of one said imager is synchronized by a  
horizontal clock and wherein said column counter is  
generated by dividing said horizontal clock by the number  
5 of bits in each said line.

7. The method according to Claim 2 wherein said row counter  
is generated by dividing said line address by said total  
lines in each said imager.

8. A method of accessing an imager array, said method  
comprising:

providing a bi-directional bus;

providing an array of imagers arranged in n rows and m  
5 columns wherein said n and m are positive integers, wherein  
each said imager is connected to said bi-directional bus,  
wherein a line of bits of any said imager is accessible by  
a line address, wherein each said imager has a Vmode input  
and an output enable input, and wherein said Vmode input  
10 and said output enable input must be enabled to allow  
accessing;

initializing a column counter, a row counter, and said  
line address to zero; and

accessing all of said array wherein said column

15 counter is multiplexed to generate a separate said output  
enable input for each said imager, wherein said row counter  
is multiplexed to generate a said Vmode input for each said  
row of said imagers, and wherein said accessing comprises  
further steps of:

20 accessing one line of one said imager  
corresponding to said line address, said column  
counter, and said row counter;

thereafter testing said column counter for  
equality to  $m-1$  wherein, if not equal, said column  
25 counter is incremented and said step of accessing one  
line is repeated and wherein, if equal, said column  
counter is reset;

thereafter testing said line address for equality  
to total lines in each said imager wherein, if not  
30 equal, said line address is incremented and said step  
of accessing one line is repeated, and wherein, if  
equal, said line address is reset; and

thereafter testing said row counter for equality  
to  $n-1$  wherein, if not equal, said row counter is  
35 incremented and said step of accessing one line is  
repeated, and wherein, if equal, said step of  
accessing all is completed.

9. The method according to Claim 8 wherein said step of  
accessing one line of one said imager is synchronized by a  
horizontal clock and wherein said column counter is  
generated by dividing said horizontal clock by the number  
5 of bits in each said line.

10. The method according to Claim 8 wherein said row  
counter is generated by dividing said line address by said  
total lines in each said imager.

11. A multiple imager array device comprising:  
a bi-directional bus;  
an array of imagers arranged in n rows and m columns  
wherein said n and m are positive integers, wherein each  
5 said imager is connected to said bi-directional bus,  
wherein a line of bits of any said imager is accessible by  
a line address, wherein each said imager has a Vmode input  
and an output enable input, and wherein said Vmode input  
and said output enable input must be enabled to allow  
10 accessing;

a first multiplexer having an input and a plurality of  
outputs wherein said input is connected to a column counter  
and wherein each said output is connected to said output  
enable input of one of said imagers; and

15           a second multiplexer having an input and a plurality of outputs wherein said input is connected to a row counter and wherein each said output is connected to said Vmode input of each said imager in one of said rows.

12. The device according to Claim 11 further comprising a divider having an input and an output wherein said input is connected to a horizontal clock signal and wherein said output is said column counter.

13. The device according to Claim 12 wherein said horizontal clock signal is divided by the number of bits in each said line of bits.

14. The device according to Claim 11 further comprising a divider having an input and an output wherein said input is connected to said line address and wherein said output is said row counter.

15. The device according to Claim 14 wherein said line address is divided by the number of said lines in each said imager.

16. The device according to Claim 11 further comprising connecting a sum of said column counter and said row counter to said input of said first multiplexer.

17. The device according to Claim 11 further comprising optics overlaying said array of imagers wherein said optics overlap to cause images on adjacent said imagers to be appear continuous.

18. The device according to Claim 11 wherein said imagers display data from multiple sources.

19. The device according to Claim 11 wherein said bi-directional bus comprises a serial data bus.

20. The device according to Claim 11 wherein said imagers comprises CMOS devices.

21. A multiple imager array device comprising:

a bi-directional bus;

an array of imagers arranged in  $n$  rows and  $m$  columns wherein said  $n$  and  $m$  are positive integers, wherein each

5 said imager is connected to said bi-directional bus, wherein a line of bits of any said imager is accessible by



a line address, wherein each said imager has a Vmode input and an output enable input, and wherein said Vmode input and said output input must be enabled to allow accessing;

10        a first multiplexer having an input and a plurality of outputs wherein said input is connected to a sum of a column counter and a row counter and wherein each said output is connected to said output enable input of one of said imagers;

15        a second multiplexer having an input and a plurality of outputs wherein said input is connected to a row counter and wherein each said output is connected to said Vmode input of each said imager in one of said rows

20        a first divider having an input and an output wherein said input is connected to a horizontal clock signal and wherein said output is said column counter; and

      a second divider having an input and an output wherein said input is connected to said line address and wherein said output is said row counter.

22. The device according to Claim 21 wherein said horizontal clock signal is divided by the number of bits in each said line of bits.

23. The device according to Claim 21 wherein said line address is divided by the number of said lines in each said imager.

24. The device according to Claim 21 further comprising optics overlaying said array of imagers wherein said optics overlap to cause images on adjacent said imagers to be appear continuous.

25. The device according to Claim 21 wherein said imagers display data from multiple sources.